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May 17, 2005
Date of Signature

Re:	Application of:	Puri et al.
	Serial No.:	09/872,582
	Filed:	June 4, 2001
	For:	Testing Implementation Suitable for Built-In Self-Repair (BISR) Memories
	Group Art Unit:	2133
	Examiner:	Cynthia H. Britt
	Our Docket No.:	1003-0558
	LSI Docket No.:	01-054

TRANSMITTAL OF BRIEF ON APPEAL

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Respectfully Submitted,

MAGINOT, MOORE & BECK, LLP

May 17, 2005

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Enclosures

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

Sir:

This is an appeal under 37 CFR § 41.31 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the final rejection of the claims 1-16 of the above-identified patent application. These claims were indicated as finally rejected in a final Office Action dated December 17, 2004. Three copies of the brief are filed herewith, together with the $500.00 fee required under 37 CFR §

41.20(b)(2). Also, please provide any extensions of time that may be necessary and charge any fees that may be due to **Deposit Account No. 12-2252**, but not to include any payment of issue fees.

(1) REAL PARTY IN INTEREST

LSI Logic Corporation is the owner of this patent application, and therefore is the real party in interest.

(2) RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to this patent application (09/872,582).

(3) STATUS OF CLAIMS

Claims 1-16 are pending in the application.

Claims 1-16 are finally rejected.

Claims 1-16 are being appealed, and are shown in the Appendix attached to this Appeal Brief.

(4) STATUS OF AMENDMENTS

Appellant has filed no amendments after receipt of the December 17, 2004, Final Office Action (the "Final Office Action").

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to the testing of semiconductor memories, and more particularly, to built-in self-repair (BISR) memories (See, e.g., Appellant's specification at page 1, lines 7-9). In one embodiment, a circuit configuration for testing a semiconductor memory includes an output register, a plurality of shift registers and means for selecting one of the plurality of shift registers for outputting digital data to the output register.

The output register is configured to receive digital data, as are the shift registers. (See, e.g., output register 41 of Fig. 2 and shift registers 11, 12 and 13 of Fig. 2). Each of the plurality of shift registers provide as serial output the digital data to be received by the output register. (See e.g., Specification at p.7, line 13 to p.8, line 10; Fig. 2; and Specification at p.8 line 20 to p.9, line 1). Each of the plurality of shift registers includes a feedback path for enabling the digital data output by each individual register of the plurality of shift registers to be input back into the same individual register in a same sequence as the digital data is output from the same individual register. (See e.g., Specification at Application at p.9, lines 1-3).

The means for selecting one of the plurality of shift registers for outputting digital data to the output register is a controlled multiplexer 51 (Specification at p.8 and Fig. 2).

Another embodiment is a method for testing a semiconductor memory that includes a step of serially outputting digital data from a shift register into an output register. (See, e.g. Specification at p.8, lines 20-23); The method also includes inputting the digital data back into the shift register in a same sequence as the digital data is output

from the shift register (See, e.g. *id.* at p.9, lines 1-3). The method further includes examining the digital data in the output register. (See, e.g. *id.* at p.9, lines 12-15).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-16 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

Claims 1-5, 8, and 11 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Abramovici et al. in "*Digital Systems Testing and Testable Design*" IEEE Press 1990 (hereinafter, "Abramovici"); and

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Abramovici.

(7) ARGUMENT

Claims 1-16 are not Indefinite

1. The Examiner's Rejection

In the Final Office Action, the Examiner alleged that the bodies of the independent claims 1 and 11 did not correspond with their preambles. The Examiner stated, "[i]t is not clear how testing is preformed by merely loading the output register and reloading the shift registers". (Final Office Action at p.3).

The Examiner voices concerns that there is "no test data applied and no criteria listed for passing or failing data", and that there is "operational verification of the memory circuit". (*Id.*)

2. The Claims do not Require the Additional Limitations Identified by the Examiner

Applicants submit that the independent claims are sufficiently definite, and that the preambles are not inconsistent with the bodies of the claims. The test under 35 U.S.C. § 112, second paragraph, is whether one of ordinary skill in the art would be able to determine the metes and bounds of the claimed property. Independent claims 1 and 11 have a readily determinable scope.

For example, claim 1 is directed to a circuit configuration for testing a semiconductor memory that includes an output register, a plurality of shift registers and means for selecting one of the plurality of shift registers for outputting digital data to the output register. The limitations of the output register, the shift register and the selection means, and there interrelationship, are readily understood. Moreover, such elements may readily form a circuit configuration for testing a semiconductor memory as claimed. Whether or not the preamble is read as a claim limitation, which in the case of claim 1 is not necessary, the scope of the entire claim is readily determined.

With respect to claim 11, the method includes ". . . outputting digital data from a shift register into an output register" and "examining the digital data in the output register". It is unclear how this could be interpreted to be at odds with the preamble, "a method for testing a semiconductor memory". Specifically, the claimed test method

includes moving data between registers, and then examining the data after it has been moved. Claim 11 clearly describes the steps of a test.

With regard to the Examiner's specific concern that there is "no test data applied and no criteria listed for passing or failing data", it is submitted that such information is not required to understand the metes and bounds of the invention. Moreover, claim 1 *does* indeed recite "output the digital data", and claim 11 does indeed recite "outputting digital data". Thus, even though a recitation of "test data" is not necessary, claims 1 and 11 appear to claim at least some "data" that is used in a "test" method or apparatus.

With regard to the Examiner's concern that there is "no criteria listed for passing or failing data", it is submitted that the evaluation of the results of the test is not a precondition for performing a test. In other words, evaluation of test *results* necessarily implies that the test has been completed prior to evaluation. By way of example, a common test in the electrical arts involves placing a voltage on a circuit input and then measuring the circuit's output voltage. The test *results* may then be evaluated, but the performance of the test itself does not require evaluation of the results, and certainly does not require an evaluation as to whether pass and fail criteria are met.

With regard to the "operational verification of the memory circuit", it is again submitted that the scope of claims 1 and 11 may readily be determined without reciting "operational verification of the memory circuit".

For the foregoing reasons it is respectfully submitted that the indefiniteness rejection of claims 1 and 11 are in error and should be reversed. Claims 2-10 and 12-16 stand rejected for the same reasons as claims 1 and 11. Because these reasons are insufficient to support an indefiniteness rejection, as discussed above, it is submitted that

the indefiniteness rejections of claims 2-10 and 12-16 are also in error and should be reversed.

Claims 1-5, 8 are Not Anticipated by Abramovici

1. Claim 1

Claim 1 recites limitations directed to

> an output register for receiving digital data;
> . . . .
> means for selecting one of the plurality of shift registers for outputting digital data to the output register.

Thus, claim 1 includes an output register that receives digital data, and a means for selecting one of the shift registers to output data to the output register. By way of non-limiting example, Fig. 2 of the Application shows multiple shift registers 11, 12, 13 that may be tested, and which controllably and selectively provide data to the output register 41 through a multiplexer 51.

2. Abramovici Does Not Include an Output Register nor Selecting Means

The Abramovici reference does not disclose all the limitations of claim 1. In the June 2, 2004 Office action, the Examiner stated that, with respect to claim 1, "Figure 10.9(a) [of Abramovici] shows a feedback register which outputs the same sequence that is reloaded back in the same sequence (page 433)." However, the Examiner fails to note where Abramovici cites other elements of claim 1. For example, Abramovici does not disclose an output register as claimed in claim 1 for use in a circuit configuration for

testing a semiconductor memory. Furthermore, Abramovici fails to disclose a selecting means as claimed.

With regard to the output register, the Examiner later alleged in the Final Office Action that "Abramovici et al. (on page 432, 10.6.1) disclose an output sequence from the shift register. As this text is describing testing and testable design of digital systems, it would follow that this output sequence would be sent to an output register." (Final Office Action at p.3). However, no support in the prior art is given that teaches that an output sequence provided to an output register in all cases in "testing and testable design of digital systems".

Moreover, even if it were inherent or obvious to provide an output register, there is no teaching or suggestion in Abramovici to include a *selecting means* that selectively provides output from one of the shift registers. As an initial matter, Abramovici is directed to a single bit registers coupled in series, in FIFO fashion. (Abramovici at Fig. 10.9(a)-(d)). As a consequence there is no need to select which register provides output. The FIFO operation dictates the output "register" as the last register in the series.

Accordingly, not only is there no disclosure or teaching of a selecting means as claimed in Abramovici, but also there would be no reason to include one.

For at least the reasons discussed above, Abramovici does not disclose all limitations of claims 1. Accordingly, it is submitted that claim 1 is allowable and the examiner's rejection of claims 1 as anticipated by Abramovici under 35 U.S.C. § 102(b) should be reversed.

Furthermore, claims 2-5 and 8 depend from and incorporate all the limitations of allowable independent claim 1. Accordingly, it is respectfully submitted that the

anticipation rejections of dependent claims 2-5 and 8 should be reversed for at least the same reasons.

Claims 6 and 7 are Not Obvious Over Abramovici

The Examiner rejected claims 6 and 7 as allegedly being obvious over Abramovici without a secondary reference. Claims 6 and 7 depend from and incorporate all the limitations of allowable independent claim 1. Accordingly, because nothing in the obviousness rejection of claims 6 and 7 addresses the deficiencies of Abramovici with respect to claim 1, it is respectfully submitted that the obviousness rejections of claims 6 and 7 should be reversed for at least the same reasons as those set forth above in connection with claim 1.

Claim 11 is Not Anticipated by Abramovici

Claim 11 recites limitations directed to

> serially outputting digital data from a shift register into an output register;
> inputting the digital data back into the shift register in a same sequence as the digital data is output from the shift register; and
> examining the digital data in the output register.

Abramovici does not disclose all the limitations of claim 11. For example, Abramovici does not disclose outputting data to an output register, nor examining digital data in an output register as claimed in claim 11 in a method for testing a semiconductor memory. Abramovici therefore fails to disclose two of the three steps of claim 11.

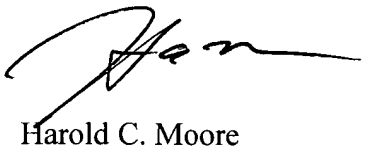
For at least the reasons discussed above, it is respectfully submitted that the rejection of claim 11 as anticipated by Abramovici under 35 U.S.C. § 102(b) should be reversed.

(8) CONCLUSION

Claims 1-16 are not unpatentable under 35 U.S.C. § 112, second paragraph, as being indefinite, claims 1-8 and 11 are not unpatentable over Abramovici. The Board of Appeals is therefore respectfully requested to reverse the rejection of claims 1-16.

Respectfully submitted,

MAGINOT, MOORE & BECK



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(9) CLAIMS APPENDIX

1. A circuit configuration for testing a semiconductor memory, comprising:

an output register for receiving digital data;

a plurality of shift registers for serially outputting the digital data to be received by the output register, wherein each of the plurality of shift registers includes a feedback path for enabling the digital data output by each individual register of the plurality of shift registers to be input back into the same individual register in a same sequence as the digital data is output from the same individual register; and

means for selecting one of the plurality of shift registers for outputting digital data to the output register.

2. The circuit configuration of claim 1, wherein each one of the plurality of shift registers has a different bit storage capacity.

3. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 48-bit register.

4. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 33-bit register.

5. The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 20-bit register.

6. The circuit configuration of claim 1, wherein the output register has a bit storage capacity equal to a bit storage capacity of a largest one of the plurality of shift registers.

7. The circuit configuration of claim 1, further comprising an output pin which is strobed to examine contents of the output register.

8. The circuit configuration of claim 1, wherein the means for selecting comprises a multiplexer interposed between the output register and the plurality of shift registers.

9. The circuit configuration of claim 1, wherein the semiconductor, memory is a built-in self repair (BISR) memory.

10. The circuit configuration of claim 1, wherein the digital data, received by the output register is divided into patterns corresponding to the plurality of shift registers.

11. A method for testing a semiconductor memory, comprising steps of:

serially outputting digital data from a shift register into an output register;

inputting the digital data back into the shift register in a same sequence as the digital data is output from the shift register; and

examining the digital data in the output register.

12. The method of claim 11, wherein the shift register is disabled while the digital data in the output register is examined.

13. The method of claim 11, wherein the semiconductor memory is a built-in self repair (BISR) memory.

14. The method of claim 11 further comprising the step of determining whether any bit errors are present.

15. The method of claim 11 further comprising the step of determining whether output from an additional register is to be output into the output register.

16. The circuit configuration of claim 1, wherein the semiconductor memory is a plurality of built-in self repair (BISR) memory and each of the plurality of shift registers is connected to one of the plurality of BISR memory.